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H. Nagano		

DEVICE SPECIFICATION for
DIGITAL DBS TUNER with LINK

MODEL NO. BS2F7HZ0169

□ CUSTOMER'S APPROVAL

DATE

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SHARP PROPRIETARY

SHARP	MODEL No. BS2F7HZ0169	SPEC No. TENTATIVE	PAGE 2 / 17
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DESCRIPTION:

This specification covers DBS tuner intended for use in Digital Broadcasting Satellites. This tuner incorporates "LINK" section that is composed of 8bit ADC, multistandard DVB-S/DVB-S2 demodulator and multistandard FEC. This tuner has DVB common interface compliant transport stream output.

[1] GENERAL SPECIFICATIONS

1-1. Receiving frequency range	950MHz to 2150MHz
1-2. Input level	-65dBm to -25dBm
1-3. Input structure	F type Female
1-4. Nominal input impedance	75 ohm
1-5. RF IC	STV6110A (write/read address: C0h/C1h) (Reference clock: Internal 16MHz crystal oscillation)
1-6. Cutoff frequency of Baseband(=I/Q out) LPF	Variable from 5MHz to 36MHz by 1MHz step
1-7. LINK IC	STV0903BAB (write/read address: D0h/D1h) (Reference clock: supplied from "STV6110A")
1-8. LNB control	DiSEqC 2.x – 22 kHz interface
1-9. Multistandard demodulation and decoding	[DVB-S] >Channel symbol rate up to QPSK 45MSps >Inner Viterbi and Outer Reed-solomon decoding >Punctured rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8 [DVB-S2] >Channel symbol rates up to QPSK 45MSps, and 8PSK 37MSps >Inner LDPC and outer BCH decoding >Punctured rates 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10 >Roll-off 0.35, 0.25, 0.20
1-10. Operating voltage	(B2, B3 and B4) 3.3V +/- 0.150V DC (VDD) 1.0V +/- 0.050V DC
1-11. Environmental characteristics	RoHS compliant (RoHS refers to the "DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.")

1-12. Attention items:

1) This unit contains components that can be damaged by electro-static discharge. Before handling this unit, ground your hands, tools, working desks and equipment to protect the unit from Electronic Static Destroy.
2) Avoid following actions;
   a) to store this unit in the place of the high temperature and humidity.
   b) to expose this unit to corrosive gases.

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[2] MECHANICAL SPECIFICATION

2-1. Dimension and mounting details	see section [14]
2-2. Mass	T.B.D.
2-3. Strength of F-connector	No severe transform or distortion at bending moment, 0.98N·m. To be connected electrically.
2-4. Clamp Torque of F-connector	No severe transform or distortion on the connection with F-connector at bending moment, 0.98N·m. To be connected electrically.

[3] ENVIRONMENTAL SPECIFICATION
(ELECTRICAL FUNCTIONAL OPERATION GUARANTEE)

3-1. Operating	Temperature	0deg.C to +60deg.C
	Humidity	Less than 85% No condensation
3-2. Storage	Temperature	-20deg.C to +85deg.C
	Humidity	Less than 95% Water vapor pressure 6643Pa max, without condensation

<Notice>
Please be careful that sudden temperature changes may cause condensation during storage, and such condensation may cause corrosion.

[4] ABSOLUTE MAXIMUM VOLTAGE

Table 1;

Pin name	Pin No.	MIN.	MAX	UNIT	Note
B1B	1		25	V	400mA max.
B1A	2		25	V	400mA max.
B4	3	-0.3	3.63	V	
B2	4	-0.3	3.6	V	
B3	11	-0.25	3.63	V	
VDD	13	-0.1	1.26	V	
I/O pins	8, 9, ...	-0.3	B3+0.3	V	

[5] TESTING CONDITION

5-1. Supply voltage

Table 2;

Pin name	Pin No.	MIN.	TYP.	MAX.	UNIT	Note
B4	3	3.25	3.30	3.35	V	
B2	4	3.25	3.30	3.35	V	
B3	11	3.25	3.30	3.35	V	
VDD	13	0.98	1.00	1.02	V	

5-2. Ambient temperature	25deg.C +/- 5deg.C
5-3. Ambient humidity	65% +/- 10%

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[6] ELECTRICAL CHARACTERISTIC (Unless otherwise stated testing condition 5-1～5-3.)

Table3;

No.	Item		Specification				Condition
			MIN.	TYP.	MAX.	UNIT	
6-1	RF input VSWR			2.0	2.5		950MHz to 2150MHz
6-2	Noise figure(at max. gain)			6	12	dB	Vagc=0.3V
6-3	2tone IM3 UD1=Fo+29.5MHz, UD2=Fo+59.0MHz			-55	-40	dBc	RFIN=-25dBm BBOUT=250mVp-p
6-4	Maximum conversion gain			65		dB	AGC=3.0V, BBGAIN=2dB
6-5	Minimum conversion gain			-30		dB	AGC=0.3V, BBGIAN=2dB
6-6	AGC range			95			
6-7	PLL settling time			50	200	us	limited to STV6110A
6-8	PLL phase noise	1kHz offset		-81		dBc/Hz	Icp=500uA
		10kHz offset		-87			
		100kHz offset		-90			
6-9	L.O. leak at RF input terminal				-70	dBm	950MHz to 2150MHz
6-10	Current consumption	B2		220	260	mA	
		B3		90	185	mA	
		B4		25	40	mA	
		VDD		400	2200	mA	
6-11	RF output VSWR			2.0	2.5		
6-12	RF output gain		-5	0	+5	dB	

[7] ERROR RATE PERFORMANCE

Table 4-1; Es/No performance at Quasi Error Free (DVB-S2 mode)

Mode	ETSI Ideal	Performance (Typical)	Unit	Note
QPSK 1/2	1.00	1.2		>DVB-S2 >Pilot: ON >BW = Symbol_rate >BERTester: SFU
QPSK 3/5	2.23	2.4		
QPSK 2/3	3.10	3.2		
QPSK 3/4	4.03	4.2		
QPSK 4/5	4.68	4.8	dB	
QPSK 5/6	5.18	5.3		
QPSK 8/9	6.20	6.4		
QPSK 9/10	6.42	6.6		
8PSK 3/5	5.50	5.8		
8PSK 2/3	6.62	6.8		
8PSK 3/4	7.91	8.1		
8PSK 5/6	9.35	9.6		
8PSK 8/9	10.69	10.9		
8PSK 9/10	10.98	11.3		

Table 4-2; E_b/N_o performance at Quasi Error Free (DVB-S mode)

Code rate	DVB-S standard (Maximum)	Performance (Typical)	Unit	Note
QPSK 1/2	4.5	3.7		>DVB-S >post Vitebi BER=$2x10^{-4}$
QPSK 2/3	5.0	4.2		
QPSK 3/4	5.5	4.7	dB	
QPSK 5/6	6.0	5.3		
QPSK 7/8	6.4	5.7		

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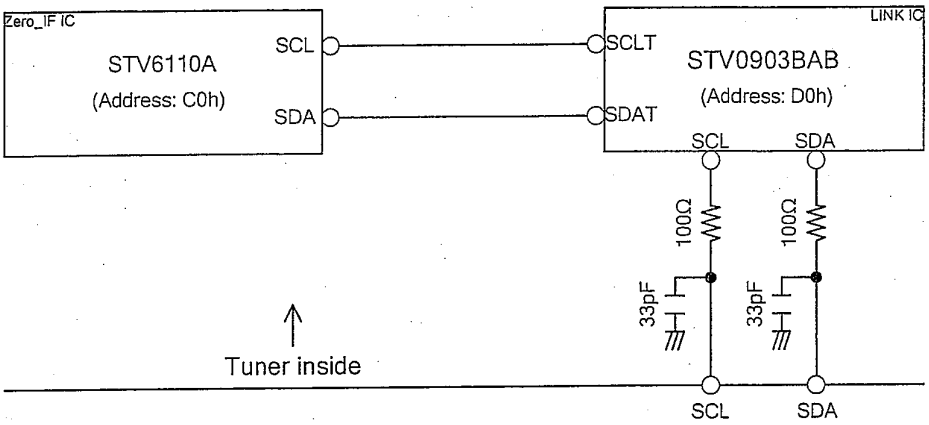
[8] I²C INTERFACE SPECIFICATION

8-1. Internal connection

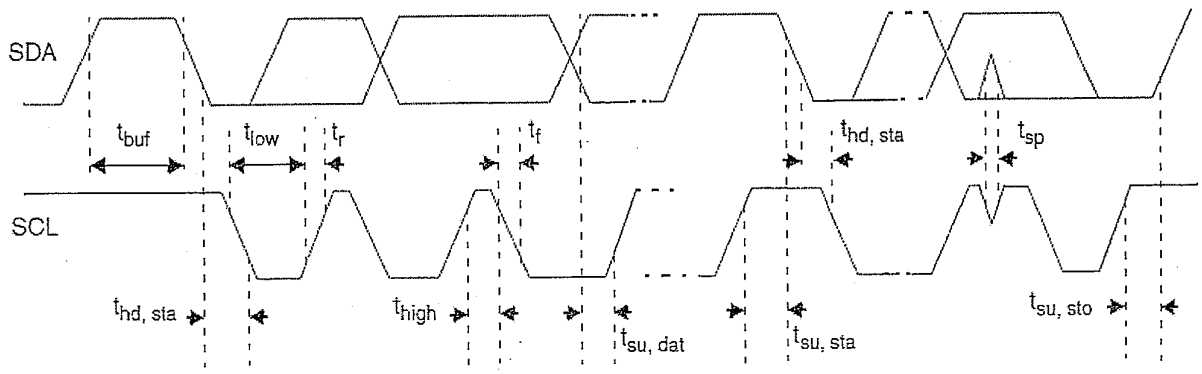
The Internal I²C connection diagram of this tuner is as following figure. It is using the I²C private repeater of STV0903BAB for tuner isolation.



8-2. I2C bus characteristic (conforms to the specification of STV0903BAB)

Table 5;

Item	Synbol	MIN.	MAX.	Unit	Note
Input high voltage	V_{ih}	2.0	3.6	V	
Input low voltage	V_{il}	-0.5	0.8	V	
SCL clock rate	f_{scl}		400	kHz	Fast mode
Bus free time between a stop and start condition	t_{buf}	1.3		us	
Hold time (repeated) start condition	$t_{hd,\ sta}$	0.6		us	After this period, the first clock pulse is generated.
Low period of the SCL	t_{low}	1.3		us	
High period of the SCL	t_{high}	0.6		us	
Rise time for SDA and SCL	t_r		300	ns	Fast mode
Fall time for SDA and SCL	t_f		300	ns	Fast mode
Setup time for a repeated start condition	$t_{su,\ sta}$	0.6		us	
Setup time for stop condition	$t_{su,\ sto}$	0.6		us	
Data setup time	$t_{su,\ dat}$	100		ns	
Pulse width of spikes to be suppressed by input filter	t_{sp}		50	ns	Fast mode



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[9] STV6110A PROGRAMMING

9-1. Tuning overview

When the PLL is locked, the frequency of the local oscillator is given by:

$$f_{LO} = N * f_{XTAL} / R / P = f_{VCO} / P = f_{LOstep} * N$$

f_{VCO}: The frequency of VCO output, set up using registers *TUNING1* and *TUNING2.*
f_{XTAL}: The frequency of crystal oscillator output
N: The division ratio of the N-integer divider, programmed in bitfield N_DIV
R: The division ratio R of the reference divider, controlled through R_DIV[1:0]
P: The division ratio P of the post divider, controlled using bit DIV4SEL.

The VCO operates from f_{VCO} = 2600 MHz to 5200 MHz. In order to generate a LO frequency (f_{LO}) from 950 MHz to 2150 MHz, the appropriate value of P has to be selected (2 or 4).
For input frequencies below 1300 MHz the P divider has to be set to 4.
For input frequencies above 1300 MHz, the P divider has to be set to 2.
To keep the step constant between all the LO frequencies (f_{LOstep}), the product of R and P must be kept constant.
For example, if fXTAL = 16 MHz, fLO = 2150 MHz and f_{LOstep} = 1 MHz then the VCO frequency could be either 4300 MHz (2 * fVCO) or 8600 MHz (4 * f_{VCO}). However, f_{VCO} must lie within the range 2600 MHz to 5200 MHz, hence P = 2.
Also, N = f_{LO} / f_{LOstep} = 2150.
The last unknown, R = f_{XTAL} / (P * f_{LOstep}) = 8.
Table 6 shows the values for bits 4 and 5 of register *TUNING2* for different RF input frequencies.

Table 6; Frequency ranges and divider register settings

RF_IN frequency (MHz)	LO divisor, P	VCO frequency	DIV4SEL	PRESC32ON
950 - 1024	4	3800 - 4092	1	0
1024 - 1300	4	3968 - 5200	1	1
1300 - 2048	2	2600 - 4092	0	0
2048 - 2150	2	3968 - 4300	0	1

After N is modified the VCO calibration must be carried out.

9-2. Calibration setting

The reference clock used by the calibration functions is 1 MHz. It is generated from the crystal oscillator by a divider which is set up in bitfield K[4:0] in register *CTRL1.*
The bandwidth calibration requires that:

f_{XTAL} / (K + 16) = 1 MHz

If the crystal frequency is fixed by the application to 16 MHz, then, K has to be set to 0.
This reference clock is used by all the calibration functions.

<<VCO calibration>>
The VCO must be calibrated after N_DIV is reprogrammed. The calibration is started by setting bit CALVCO_STRT = 1 in register *STAT1.* It runs automatically. After the settling time of the synthesizer, the chip writes 0 into CALVCO_STRT to indicate that the calibration is completed.

<<LPF calibration>>
The low-pass filter cut-off frequency must be calibrated after CF[4:0] is reprogrammed. The calibration is started by setting bit CALRC_STRT = 1 in register *STAT1* and it runs automatically. To indicate the calibration is completed, the chip writes 0 into the CALRC_STRT.

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9-3. Registers

The registers are automatically reset to their default values at power up by a power-on-reset (POR).

Table 7;

Name	Addr	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTRL 1	0x0	0x5F	K[4:0]					LPT	RX	SYN
CTRL 2	0x1	0x33	CO_DIV[1:0]		1	REFOUTSEL	BB_GAIN[3:0]			
TUNING0	0x2	0x30	N_DIV[7:0]							
TUNING1	0x3	0xC7	R_DIV[1:0]		PRESC32ON	DIV4SEL	N_DIV[11:8]			
CTRL 3	0x4	0x12	DCLOP_OFF	0	ICP	CF[4:0]				
STAT 1	0x5	0x06	Reserved for test: set to 0					CALVCO_STRT	CALRC_STRT	LOCK
STAT 2	0x6	0x00	Reserved for test: set to 0							
STAT 3	0x7	0x00	Reserved for test: set to 0							

K[4:0]: determines the divider value for setting the calibration frequency (see *Section 9-2.*). The application requires a calibration frequency of 1 MHz.

LPT, RX, SYN: These three bits set the operating level. Only four combinations are allowed as given in the table below:

LPT	RX	SYN	Operating levels		
			Loop-through	Synthesizer (VCO, PFD, CP, Dividers)	LNA, Mixer, LPF, PGA and Buffers
0	0	0	Off	Off	Off
1	1	1	On	On	On
0	1	1	Off	On	On
1	0	0	On	Off	Off, except the LNA
All other combinations			Reserved: not to be used		

CO_DIV[1:0]: sets the crystal oscillator divisor value, CO, for the output clock:

00: divide by 1 (output frequency is f_{XTAL}) (default)
01: divide by 2
10: divide by 4
11: divide by 8

REFOUTSEL: sets the DC voltage on pins IP, IN, QP, QN:

0: VCC / 2
1: 1.25 V (default)

BB_GAIN[3:0]: sets the baseband amplifier gain. When the amplifier is on, the gain is increased as follows:

0x0: 0 dB
0x1: 2 dB
0x2: 4 dB
0x3: 6 dB (default)
0x4: 8 dB
0x5: 10 dB
0x6: 12 dB
0x7: 14 dB
0x8: 16 dB
0x9-0xF: not used.

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N_DIV[7:0]: the LSBs of N_DIV[11:0], which sets the N-integer divider value, N.

N_DIV[11:8]: the MSBs of N_DIV[11:0], which sets the N-integer divider value N.

R_DIV[1:0]: sets the divisor, R, for the reference divider:
- 00: 2
- 01: 4
- 10: 8
- 11: 16 (default)

PRESC32ON: selects the divisor for the pre-scaler divider:
- 0: 16 (default)
- 1: 32

DIV4SEL: selects the divisor, P, for the post divider:
- 0: 2 (default)
- 1: 4

DCLOOP_OFF: selects the DC offset compensation loop:
- 0: compensation disabled (default)
- 1: compensation enabled

ICP: sets the value of the charge pump current:
- 0: 500 µA (default)
- 1: 1.0 mA

CF[4:0]: sets the baseband filter cut-off frequency:

0x00: 5 MHz	0x01: 6 MHz
0x02: 7 MHz	0x03: 8 MHz
0x04: 9 MHz	0x05: 10 MHz
0x06: 11 MHz	0x07: 12 MHz
0x08: 13 MHz	0x09: 14 MHz
0x0A: 15 MHz	0x0B: 16 MHz
0x0C: 17 MHz	0x0D: 18 MHz
0x0E: 19 MHz	0x0F: 20 MHz
0x10: 21 MHz	0x11: 22 MHz
0x12: 23 MHz (default)	0x13: 24 MHz
0x14: 25 MHz	0x15: 26 MHz
0x16: 27 MHz	0x17: 28 MHz
0x18: 29 MHz	0x19: 30 MHz
0x1A: 31 MHz	0x1B: 32MHz
0x1C: 33 MHz	0x1D: 34 MHz
0x1E: 35 MHz	0x1F: 36 MHz

CALVCO_STRT: automatic calibration of VCO:
- 0: VCO calibration finished
- 1: start VCO calibration (default)

CALRC_STRT: automatic calibration of the low-pass filter:
- 0: filter calibration finished
- 1: start filter calibration (default)

LOCK: indicates when loop is locked:
- 0: not in lock
- 1: locked

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[10] Reliability

10-1. High temperature high humidity load (40deg.C, 90% RH, 500h)
1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After cycling DUT in the constant chamber at 40deg.C/90-95% RH in on state, for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 17.

10-2. High temperature load (70deg.C, 40% RH, 500h)
1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant chamber at 70+/-2deg.C/40% RH for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 17.

10-3. Cold test (-25deg.C, 500h)
1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant temperature chamber at -25deg.C for 500h, leave the DUT at room temperature and humidity for 2h and then measure the values after test.
3) Must meet the specifications of Table 17.

10-4. Shock (686 m/s^2, 6 planes, 3 times)
1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the shock tester, apply shock of 686 m/s^2 three times to each of 6 planes and then measure the values.
3) Must meet the specifications of Table 17.
4) This test is to be conducted using a single tuner.

10-5. Vibration (10-55 Hz, 1.5 mm, in each of three mutually perpendicular directions, each 2 times)
1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the vibration tester, apply motion having an amplitude of 1.5 mm (constant), the frequency being varied uniformly between 10 and 55 Hz, to DUT, for 2h in each of three mutually perpendicular directions (X, Y and Z, total of 6h). After the test, measure the values.
3) Must meet the specifications of Table 17.
4) This test is to be conducted using a single tuner.

10-6. Heat shock test (1 cycle=1h (-20deg.C; 0.5h, 70deg.C;0.5h), 50 cycles))
1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) Using the heat shock tester, apply heat shock to DUT. After the test, measure the values.
3) Must meet the specifications of Table 17.

10-7. Solderability of terminal

Pretreatment of heating terminal at 150deg.C for 1h is performed and leave it at room temperature for 2h or longer. Immerse 1.9 mm length of terminal (from the tip) to be soldered into rosin (JIS-K-5902), isopropyl alcohol (JIS-K-8839 or JIS-K-1522, rosin concentration (10-35% range) approx. 25% by weight unless otherwise specified) or equivalent solution for 3–5s, and then immerse the length of the terminal into a pool of molten solder (Sn/3.0Ag/0.5Cu, or equivalent) at 240 +/-2deg.C for 3s.Dipped terminal portion shall be wetted by more than 95%. (Excluding the cutting plane of the chassis)

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10-8. Soldering heat resistance

Immerse the terminal mounted on a PCB (1.6t thick) into solder at 350±5deg.C for 3.0-3.5 seconds or at 260 +/-5deg.C for 10 +/-1 seconds. Remove the PCB from the solder and leave it for 1 hour at room temperature. The test sample shall show no degradation in appearance and electrical characteristics.

10-9. ESD protection

Table 16; ESD Test Condition (IEC61000-4-2 Compliant)

Terminal	Limits	Condition
RF_IN (coaxial center)	+/-6kV DC	150pF/330ohm each 5 times
Others	+/-200V DC	150pF/330ohm each 5 times

10-10. Judgment

Table 17; Specification after the reliability tests

Item		Spec.	UNIT	Condition
Current consumption	B2	< 300	mA	3.3V
	B3	< 185	mA	3.3V
	VDD	< 2200	mA	1.0V
Es/No at QEF	8PSK 3/4	< 8.2	dB	DVB-S2, Pilot: ON

Note) All TS outputs are checked with SFU. Other I/O pins are checked with oscilloscope.

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[11] BLOCK DIAGRAM

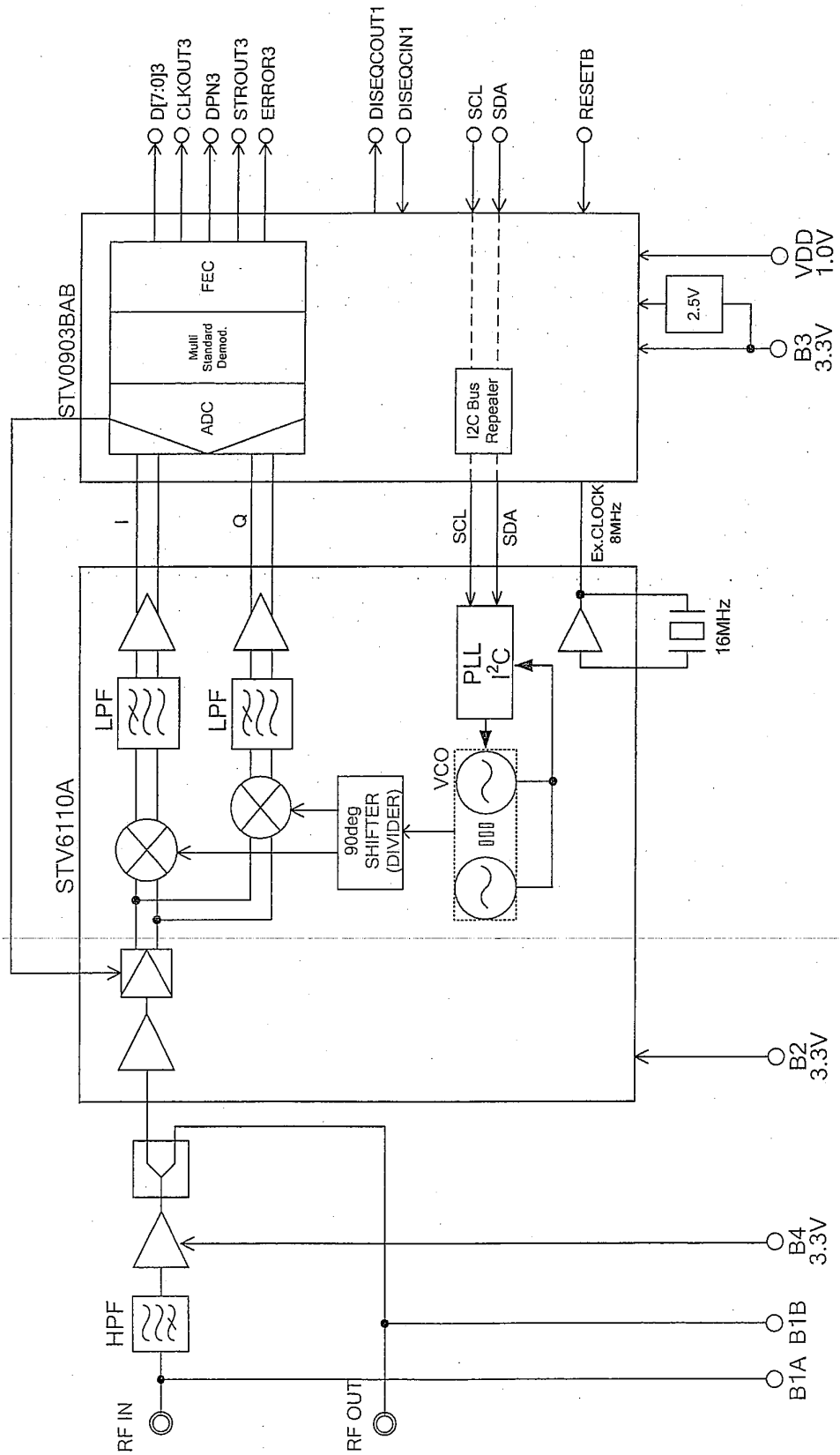

Fig 1. BLOCK DIAGRAM

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[12] PIN LIST

No.	NAME	LOGIC	PIN DESCRIPTION
1	B1B		Voltage supply of LNB B. Please ground it with a 1000pF ceramic capacitor.
2	B1A		Voltage supply of LNB A. Please ground it with a 1000pF ceramic capacitor.
3	B4		3.3V supply for RF booster amp.
4	B2		3.3V supply for STV6110. Please keep a ripple at the Power Supply less than 10mVp-p.
5,6,7	NC		It is not connected inside the unit.
8	SDA	3.3V	I^2C Bus. Please connect a pull-up resistor which is more than 2k ohm outside of the tuner.
9	SCL	3.3V	
10	DISEQCIN1	3.3V	DiSEqC 1 input
11	B3		3.3V supply for STV0903. It is internally converted into 2.5V.
12	DISEQCOUT1	3.3V	DiSEqC 1 output.
13	VDD		1.0V supply for STV0903.
14,...,21	D03,...,D73	3.3V	Transport stream 3 data.
22	CLK_OUT	3.3V	Transport stream 3 clock out.
23	D/PN	3.3V	Transport stream 3 data parity.
24	STROUT	3.3V	Transport stream 3 sync.
25	ERROR	3.3V	Transport stream error.
26	RESETB	3.3V	Chip reset active low.

Note: The 3.3 V digital I/Os comply to the JEDEC standard JESD8b.

Note: It is recommended, where possible, to provide the following power sequencing order:
3V3 Supply powered first
1V0 Supply power last
There is no firm time delay between power supply ramp up. However, applying power sequentially, when the previous supply reaches 90% of its final voltage, is recommended.

Note: Pin RESETB, the chip reset, must remain active (low) until at least 3 ms after the last power supply has stabilized.

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[13] CONNECTION DIAGRAM FOR EVALUATION

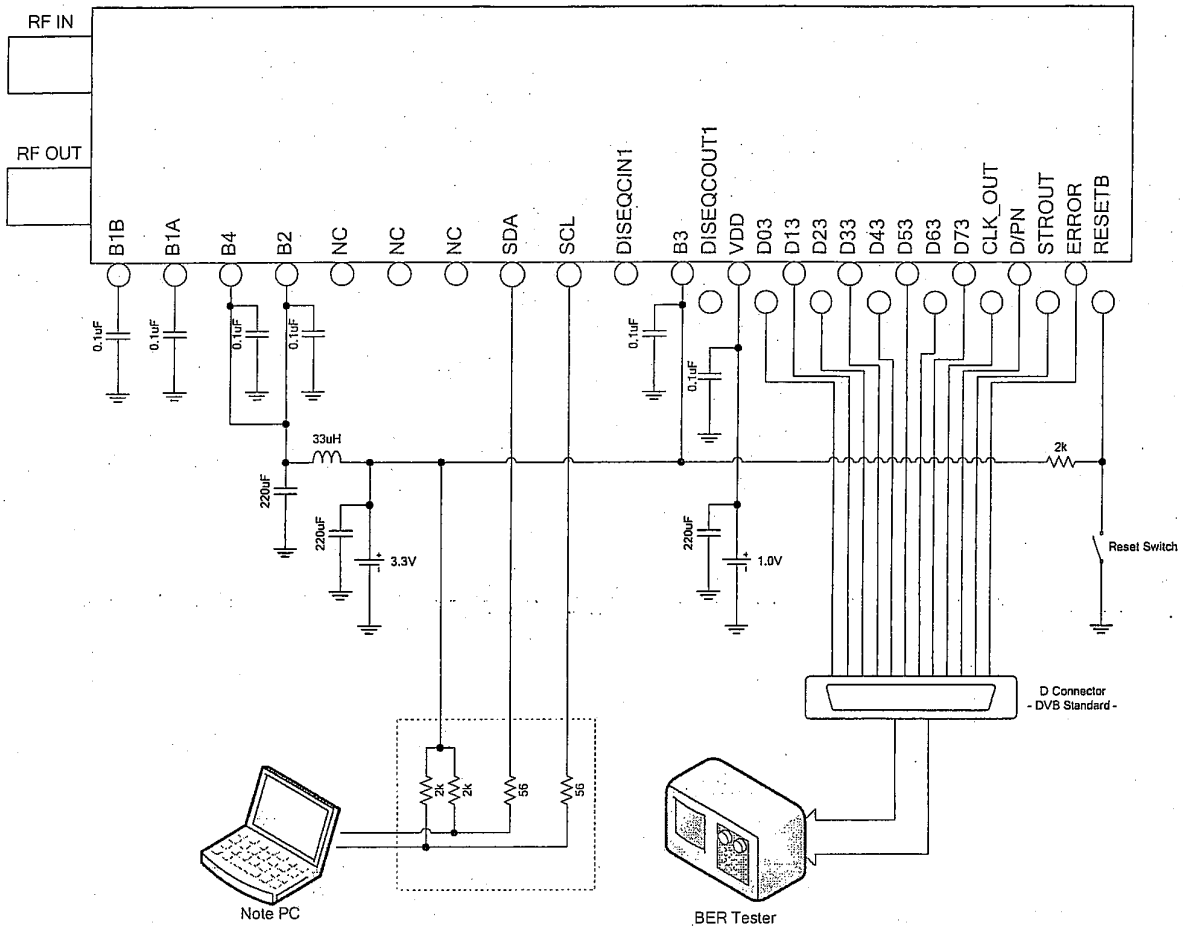

Fig 2. CONNECTION DIAGRAM

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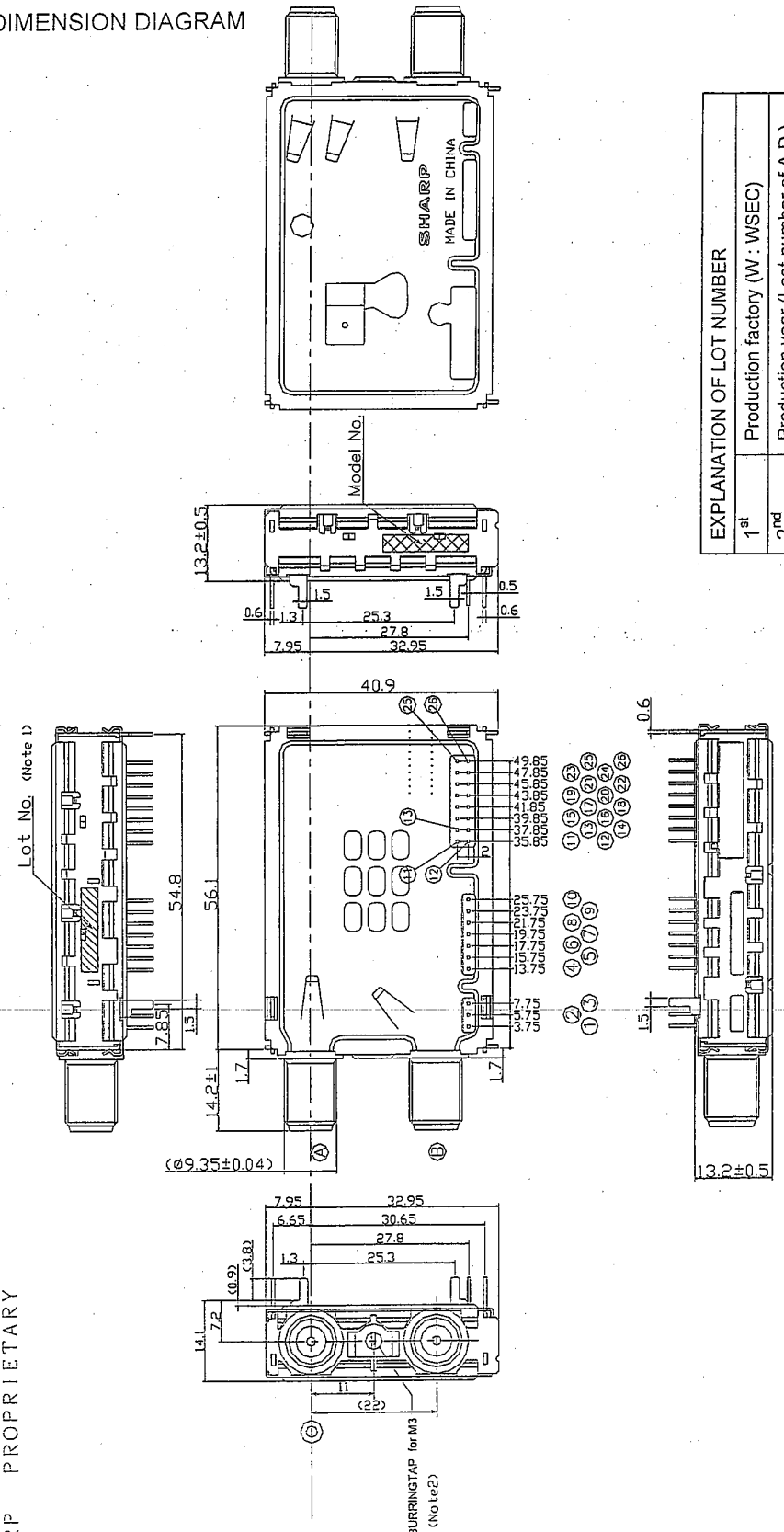
[14] DIMENSION DIAGRAM



EXPLANATION OF LOT NUMBER	
1st	Production factory (W : WSEC)
2nd	Production year (Last number of A.D.)
3rd	Production month (1, 2, 3, ...,9, O, N, D)
4th, 5th	Production day (01, 02, 03, ..., 31)
6th	History of alteration (A, B, C, ...)
7th	Production line and group of workers

Tolerances : ±0.3
Unit : mm

Note1 : The first letter of lot number "W" means made in China.
This tuner is made in China.

Note2 : The length of screw(inside of tuner) should be less than 2mm.

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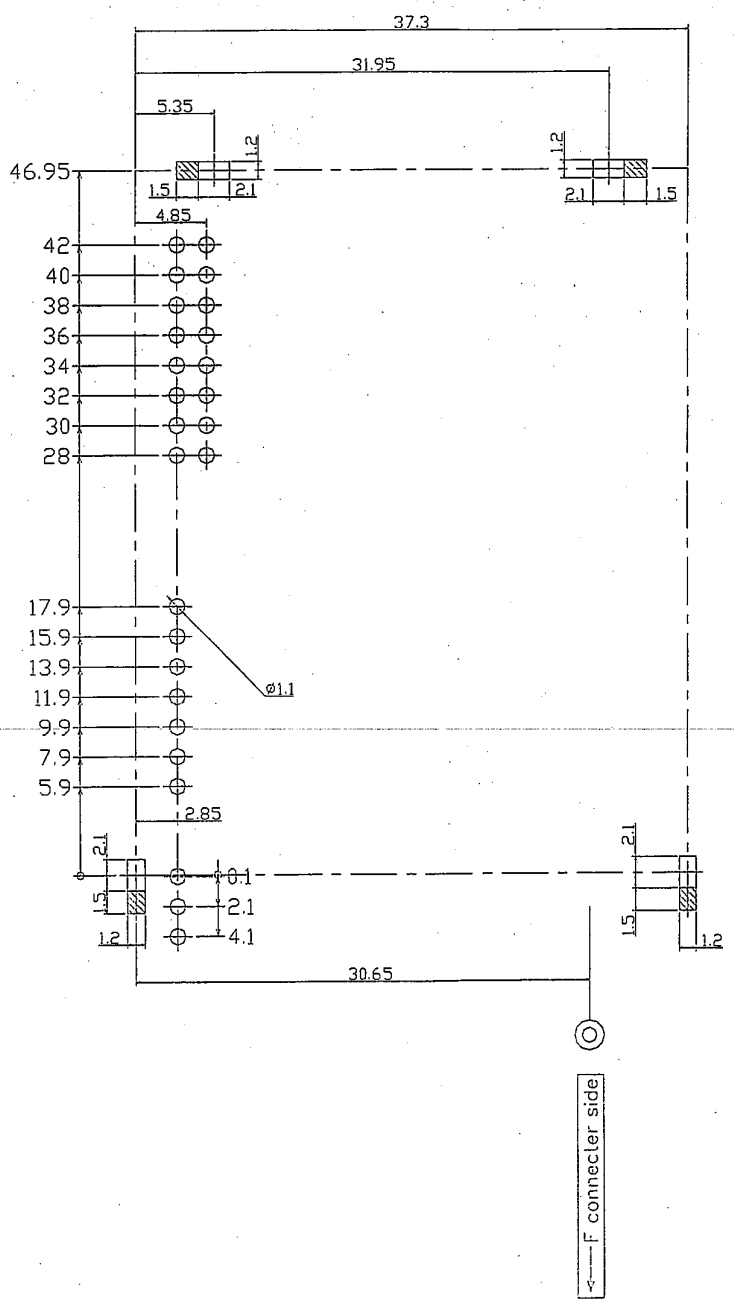
[15] MOUNTING DETALIS

Unit : mm



Recommended dimension of pin holes on mother PWB.
(Viewed from mounting side)
– Reference drawing –

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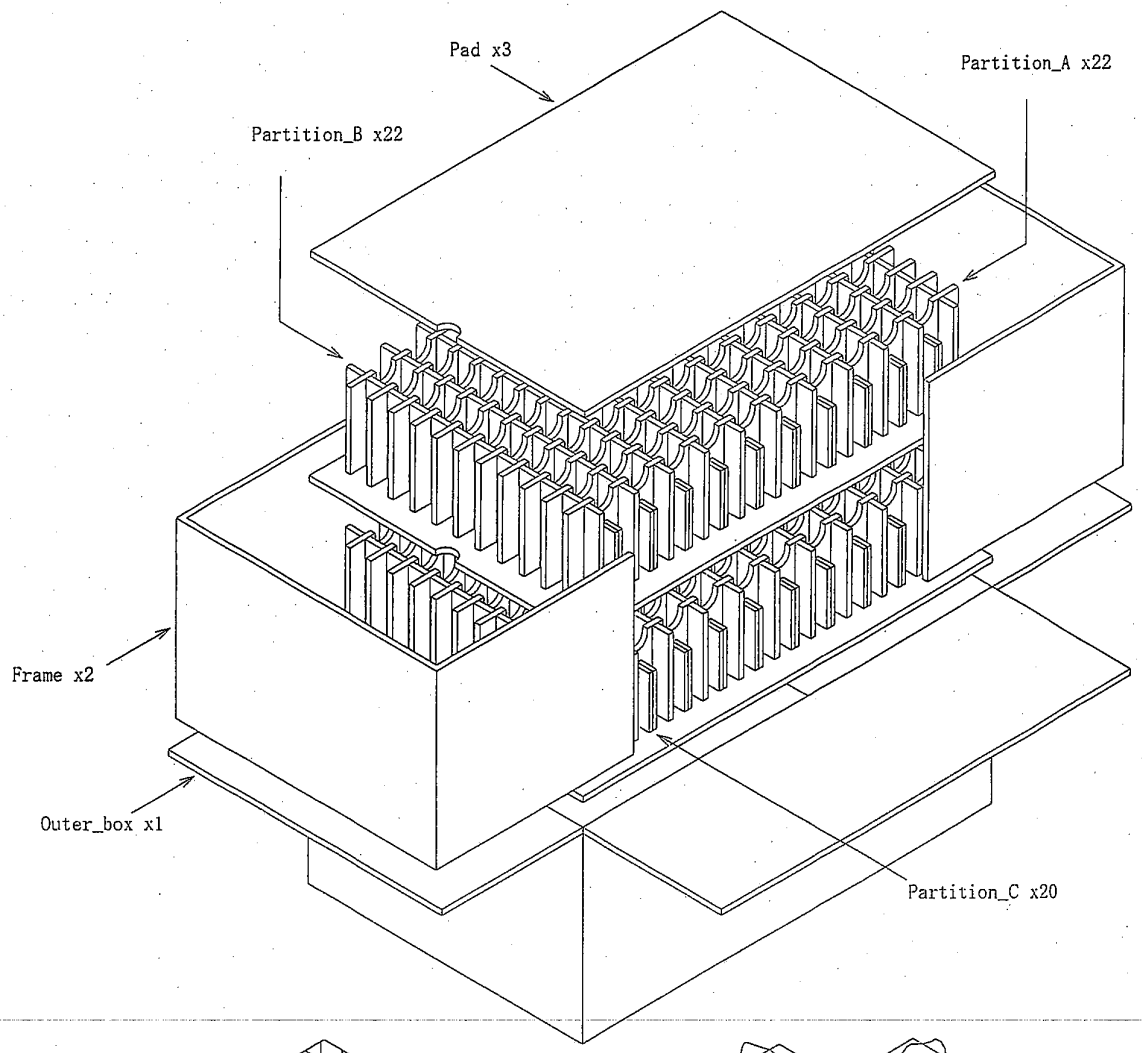
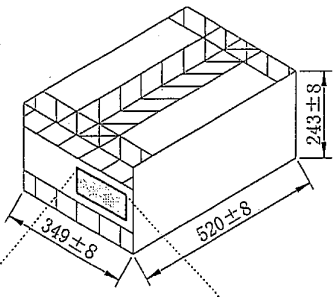
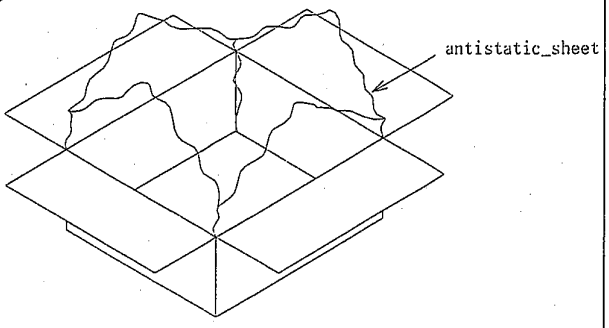
[16] PACKAGEING DETAILS







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